The Pad Chambers (PC)

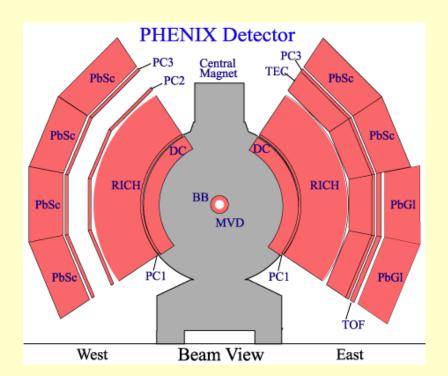
Anders Oskarsson Lund Univ.

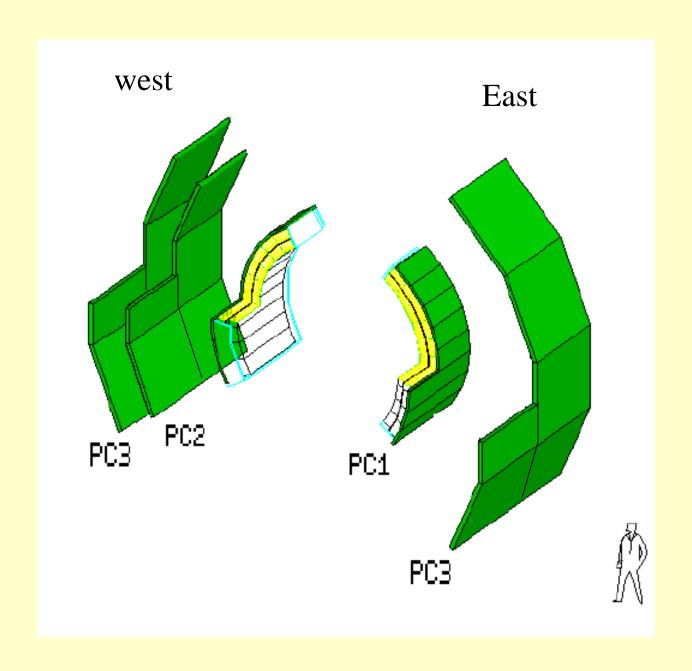
On behalf of the groups at

BNL Lund ORNL SunySB-C Vanderbilt U Weizmann Inst.

PCs role in PHENIX

- •Straight line tracking by space points
- •Z-coord from PC1
- •Pattern in 3D
- •Verify tracks thru arm for safe part. ID.
- •Charged particle veto in front of EmCal
- •Entrance/exit points (RICH,EmCal) for Lvl2 trigger





Problem: tracking at high Multiplicity. Design $dN/d\eta=2000$ Double Hijing (gives 700 in central arms).

Basic Instincts:

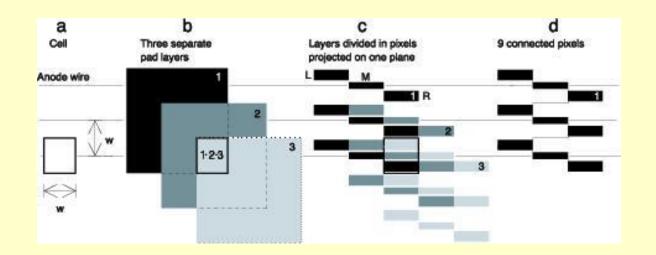
- •Resolve in 3D by space points
- •If 100% eff
- •pos resolution and 2-track separation much better than average track dist
- •then 3 points on a straight line makes it

Basic idea:

- •make a lot of small readout cells with low resolution readout instead of the normal in HEP, large cell with high resolution readout to get the pos. resolution.
- •Solve the problem of putting FEE in the fiducial volume

What you gain:

- •Low input capacitance
- •Low rate, simpler analog design
- •Low power
- •Simple A-D conversion
- •Small data volume
- •1-2\$ per ch. instead of \$50



Pixel readout:

- •3 adjacent channels (pads) fire for each hit
- •Each cell has unique triplet of channels
- •14400 cells per m² on PC1.
- •Same $d\Omega$ in PC1,2,3 (angular resolution).
- •Reconstruct to center of cell or between 2 cells
- •Saves factor 3 compared to readout of cells.
- •Occupancy ~1% in central AuAu

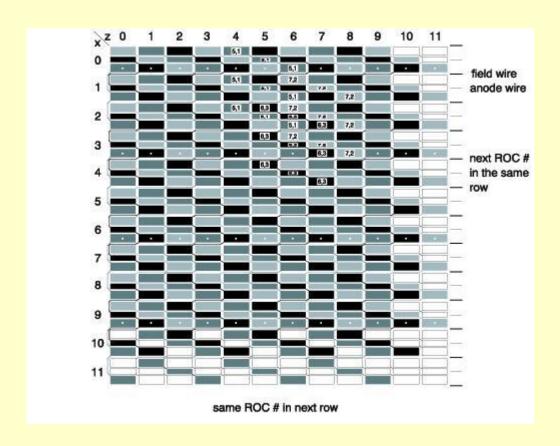
Example:

- •Electrons drift to wire →avalanche signal
- •Charge shared between pads in the cell
- •Pad areas chosen to get 1/3 charge each
- •If hit is central in cell along wire (pos A):
- •If hit is between 2 cells (pos B):



Cell deThe copper pac					deThe copper pad	
	Z = 0	Z = 1	Z = 2	Z = 3	The copper pad	
[1, -1	2, 1	3, 0	4, -1		
wire = 0	0,0	1, -1	2, 1	3, 0		
	-1, 1	0, 0	1, -1	2, 1		
	1, 2	2, 1	3, 0	4, 2		
wire = 1	0,0	1, 2	2, 1	3, 0		
	-1, 1	0, 0	1, 2	2, 1		
	1, 2	2, 1	3	4, 2	1	
wire = 2	0,3	1,2 B	A	3, 3		
	-1, 1	0,3	, 2	2, 1		
	1, 2	2, 4	3, 3	4, 2	I \	
wire = 3	0,3	1, 2	2, 4	3, 3	1	
	-1, 4	0, 3	1, 2	2, 4	\	
F D C B C C B C C B C C C C C C C C C C C						

Whatabout the edges?



Cut away pixels that have no neighbour. Works as well at the edges as in the interior. We have edges between all FEMs So, everything needed to reconstruct contained in One FEM-DCM chain. Great for LVL2.

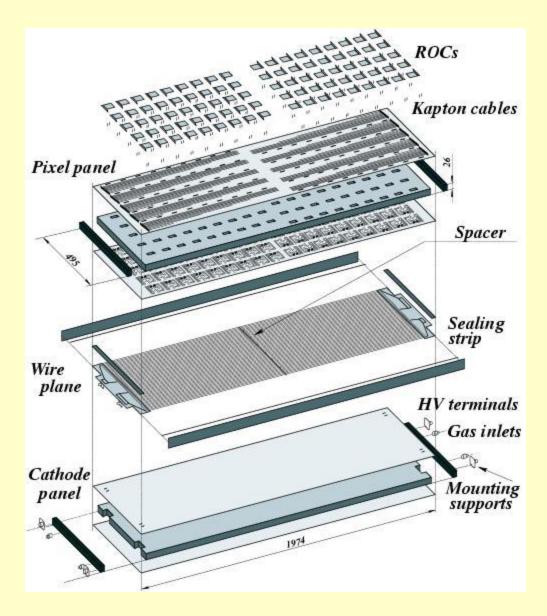


The etched copper cathode PC3 size.

Large area 1m*2m PC3 board with very fine traces and gaps.

Hit resolution limit of CAD programs.
Difficult to make.

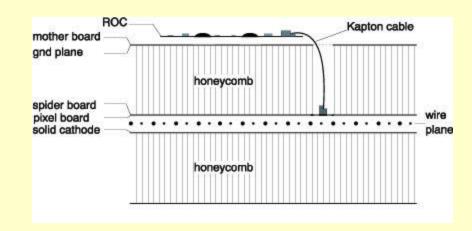
PC1, mech. Comp. from WI



Weight 7kg

Chamber construction:

- •MWPC
- •PC1 No frame in fiducial volume.
- •PC2/3 Thin Frame for gas seal.
- •Wire tension held by Honecomb sandwich
- •Ar/Ethane 50/50 flammable gas



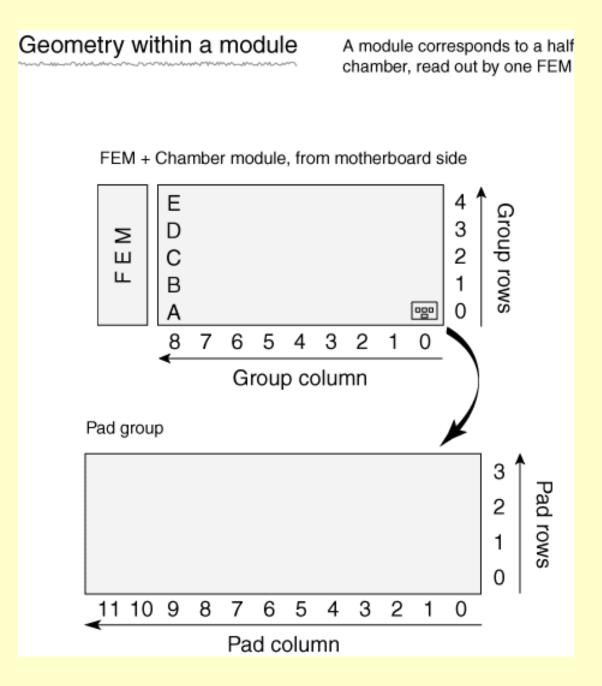
chamber	Wire dist (mm)	gas gap (mm)	Pixel length (mm)	Rad. Thickn.
PC1	8.4	6	8.4	1.2%
PC2	13.6	10	14.2	2.4%
PC3	16.0	12	16.7	2.4%

Geometry the same everywhere.

Only size is different.

Same software all over PCs for local coordinates

Everything to same FEM

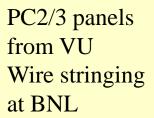


PC1, East arm [1] as viewed from IP			PC3, East arm [1] as viewed from IP				
FEM id	North side [1]	South side [0]	FEM id	FEM id	North side [1]	South side [1]	FEM id
7	Sub sector 7		7	7			7
6	Sub sector 6		6	6	Sector 3		6
5	Sub sector 5		5	5			5
4	Sub sector 4		4	4	Sector 2		4
3	Sub sector 3		3	3			3
2	Sub sector 2		2	2	Sector 1		2
1	Sub sector 1		1	1			1
0	Sub sector 0		0	0	Sector 0		0

Length scale on PC3 is twice that of PC1. Double distance Means same angular resolution

Chamber assembly in 820

A little prayer can not harm



Wire support

Frame with O-ring

No, the canadian says.

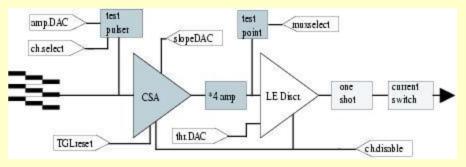
We're gonna make it

without supernatural help

Readout electronics

TGLD ASIC:

- •16ch amp/discr
- •2fC thresh, min
- •Testpulsing of ch.
- •Remote serial CTRL



ORNL design Lund testing

Lund

+SiCon

One channel TGLD

clock driven event driven clock ev 0 logic 48 deby mem0 TGLD1 out 48 *32 TGLD1 ref Current receivers TGLD2 out OR between event slices serial out TGLD2 tef TGLD3 out TGLD3 ref deby mem 1 48 * 32 write adr counter ctil readout event. transf logic level 1 memory ettot tead depth length flag event Sisteps

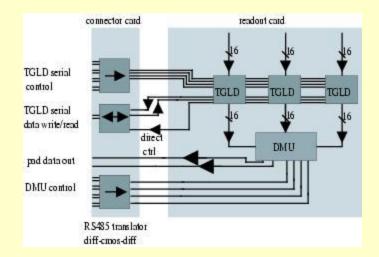
48 channels in one DMU

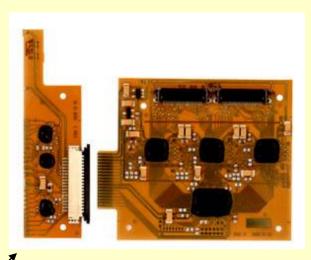
DMU ASIC:

- •48ch delay mem.
- •5 event mem.
- •Parallel in serial out
- •Serves 3 TGLD

Readout electronics

The ROCs



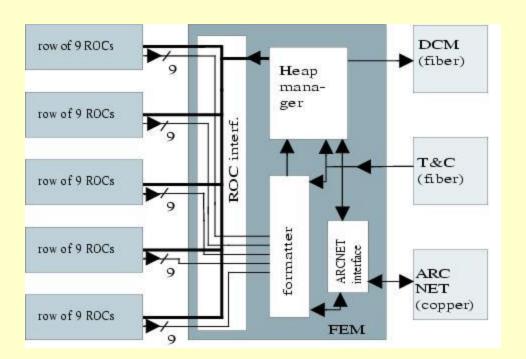


Lund +Xicon

Connector card soldered to Motherboard (top skin of pixel honeycomb sandwich.)

A ROC/conn card:

- •3 TGLD chips
- •1 DMU chip
- •48 channels
- •Diff-CMOS transl.
- •Chip on Board assembly
- •Conductive glue for components
- •Local voltage regulation.
- •0.2% of χ_0 on PC1
- •~\$75 per ROC incr. Cost
- •5000 made, 3600 used



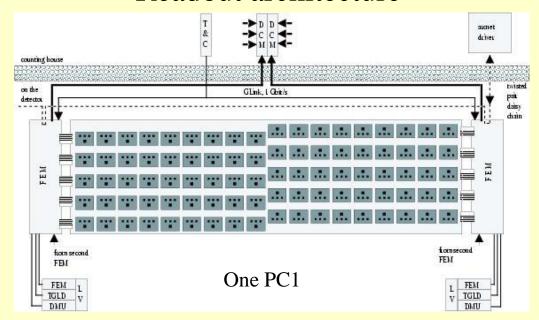


The FEM:

- •Serial control of TGLD
- •PWR distribution to ROCs
- Data readout from DMUs
- •Data formatting
- •Data transfer by Glink 800Mbit/s
- •Timing and mode control

ORNL + SB

Readout architecture



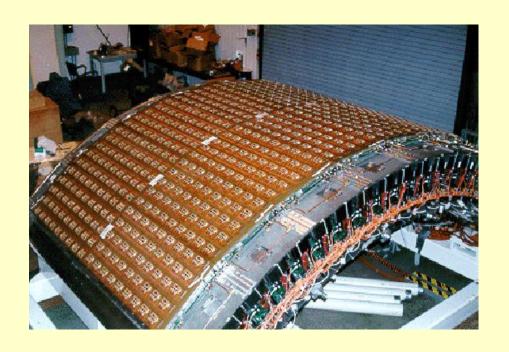
Handling an event.

- •48+3+1 ticks (all ROCs to FEM)
- •Formats to 108, 20 bit words
- •Each word is 20 pad across
- •Word number Z-coordinate
- •Bit number is x-coordinate
- •Bitwise .AND. word i-1,i,i+2 for cell
- •Zero supp, skip 20 bit words if zero
- •Average 4-5 word per hit.

Readout of one chamber:

- •2 FEMs (PC2,3 side by side)
- •Multiplexed readout (same side)
- •Identical readout for all FEMs
- •3 fibers and 1 twist pair per chamber

PC1 on DCh

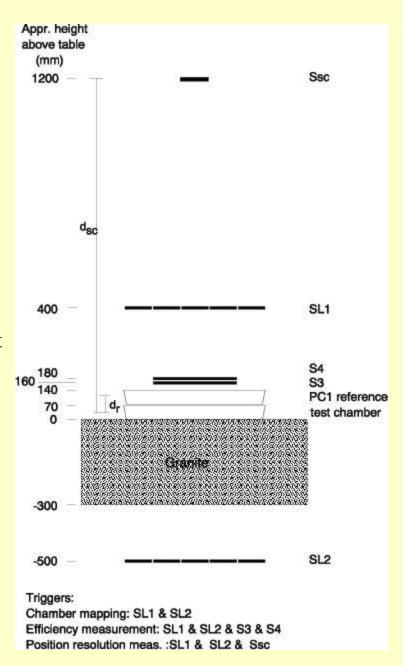


- •Five planes: East PC1,3 & WEST PC1,2,3
- • $\Delta \phi = 90^{\circ}, |\eta| = 0.35$
- •80m² MWPC, pixel cathode readout,
- •172800k readout channels,
- •1.2% χ_0 (PC1) with electronics on back

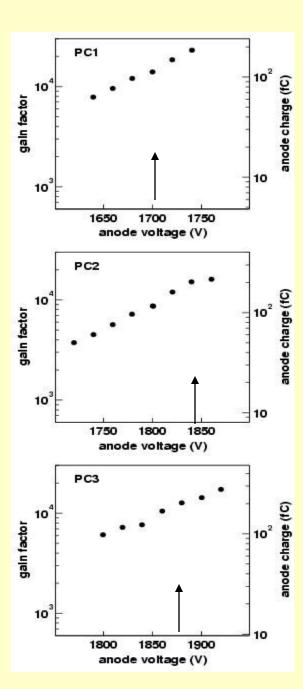
The cosmic test stand.

4 fold coinc for efficiency

Large area tested, not only sweetspot



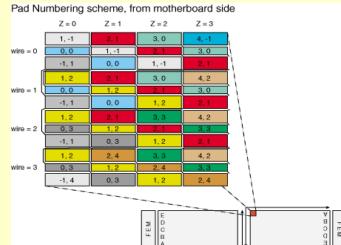
Gain curves
Running at 1-2*10⁴

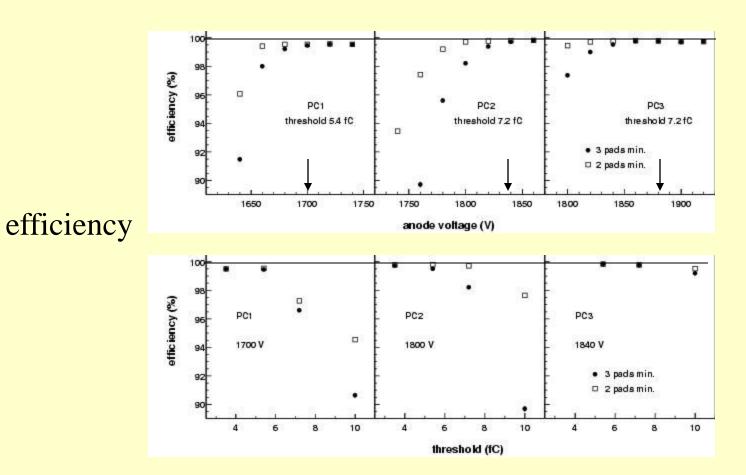


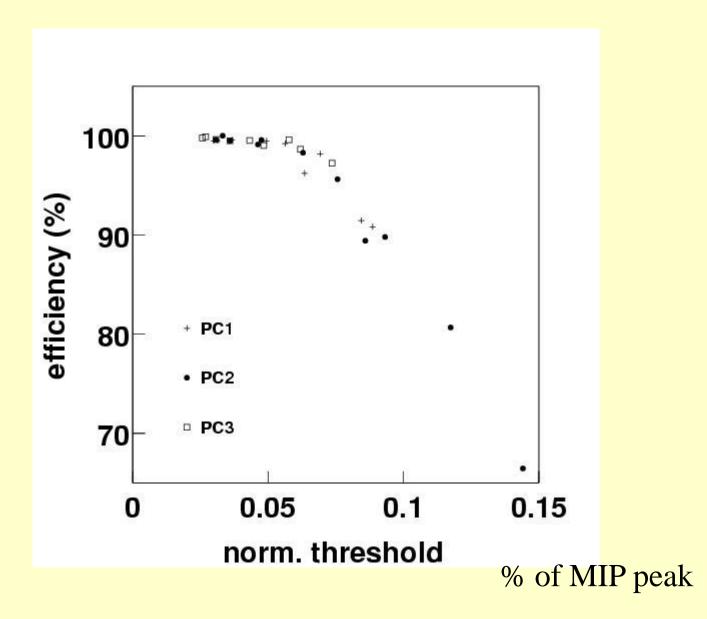
1640 V 1660 V 1680 V 0.4 frequency 0.1 1700 V 1720 V 1740 V 0.3 0.2 0.1 2 2 10 0 10 0 number of pads/hit

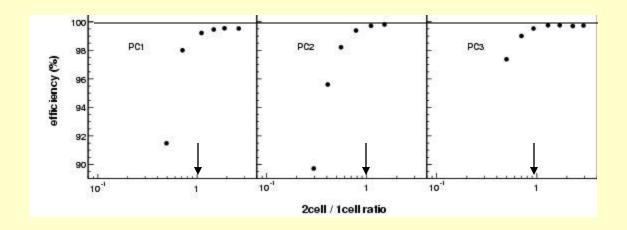
Pad multiplicity distribution per hit

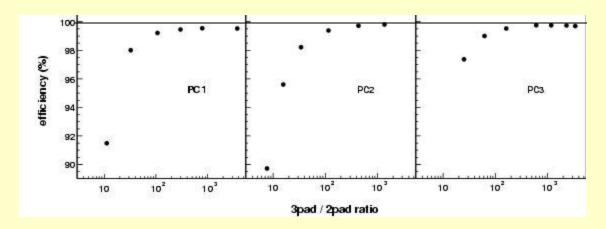
Always 3 or more when full efficiency

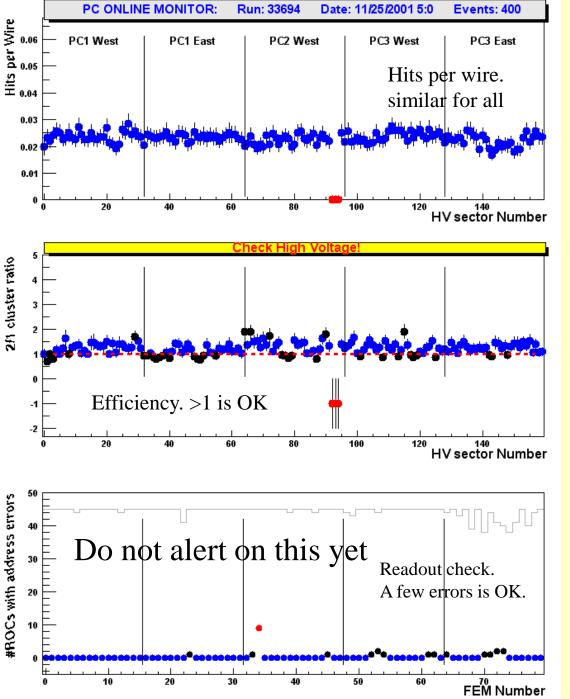


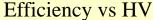


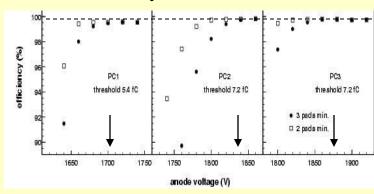


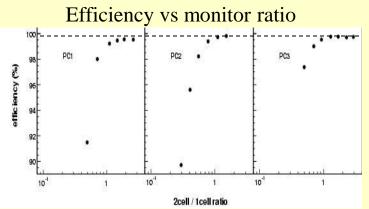










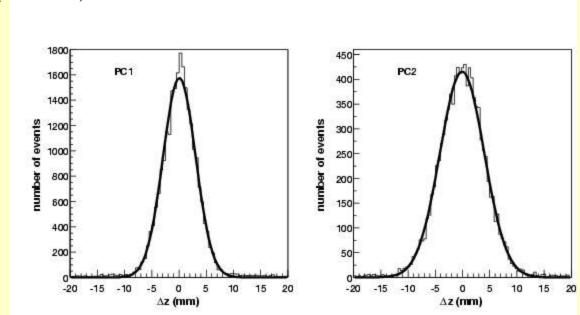


- •If red, follow the instr.
- •1 Hv-sector is one channel
- •8 channels is one bulk supply
- •Most trips are:1 or 8 channels
- •Readout check is under eval.
- •Wait for enough statistics.

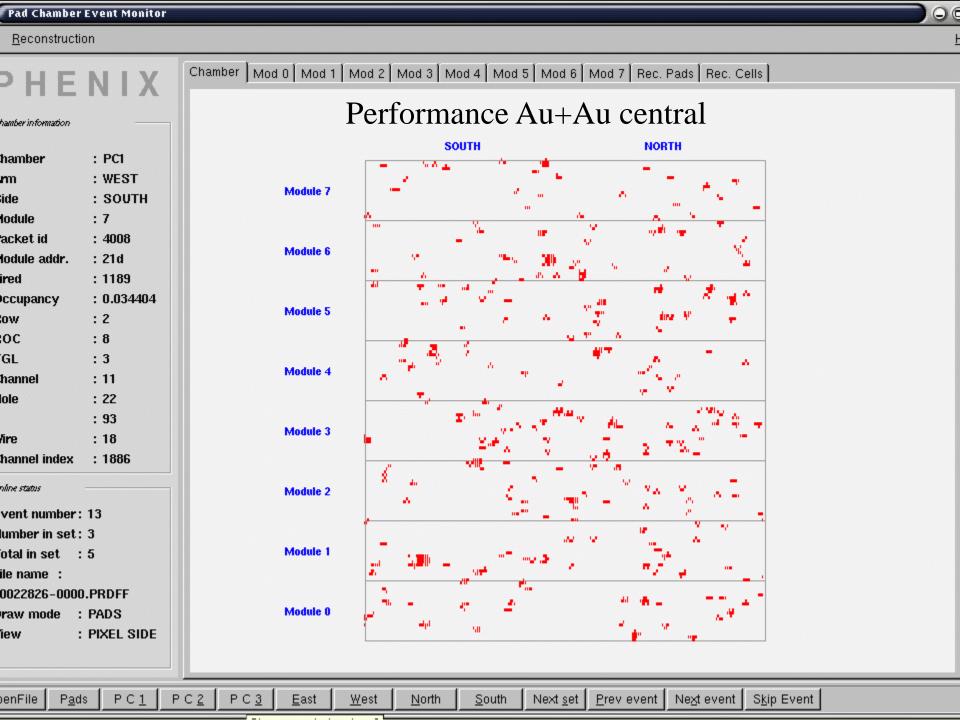
Position resolution in Z

(cosmics)

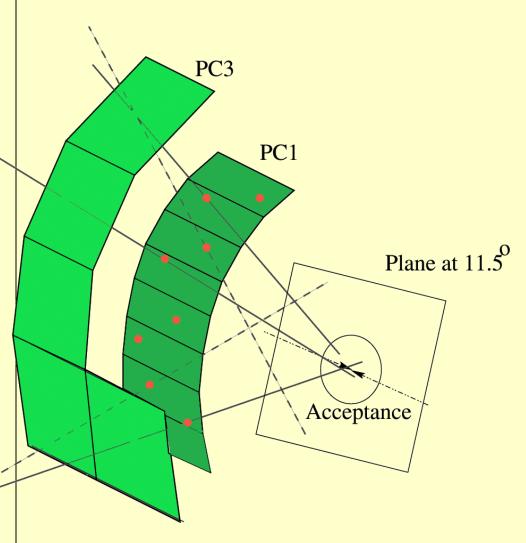
measured



chamber	Wire dist	Z-resol.	Perp res	Rad.
	(mm)	(mm)	(mm)	Thickn.
PC1	8.4	1.7	2.5	1.2%
PC2	13.6	3.1	3.9	2.4%
PC3	16.0	3.6	4.6	2.4%



Hit Matching Procedure



The analysis presented here was performed with field off runs only and using PC1 and PC3 in the East arm. (For year-2: also West arm)

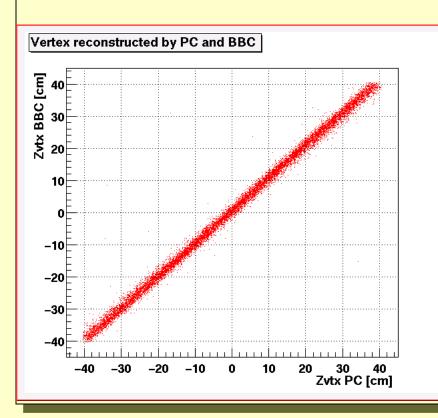
The background contribution is determined by a mixed event technique of exchanging each PC1 sector with its neighbour.

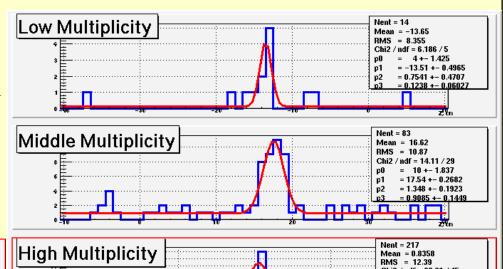
Vertex reconstruction is done by PC/BBC.

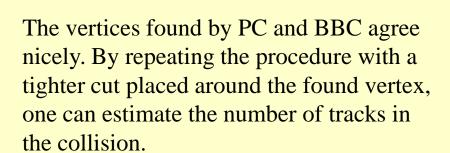
Vertex Reconstruction

The vertex position is determined by

- 1) Combining all PC1 and PC3 hits to lines
- 2) Project the lines to the plane and save all within an appropriate X and Y window.
- 3) Calculate the peak position of the Z distribution.



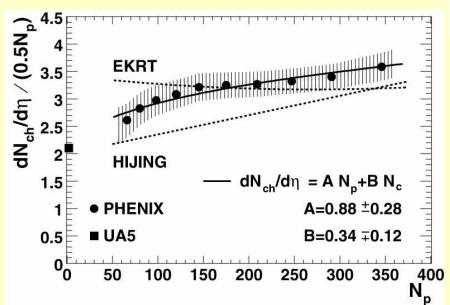


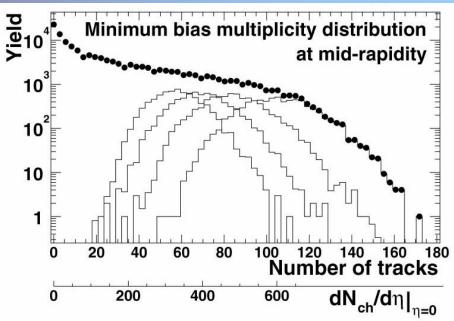


Multiplicity distribution @ 130 GeV

Distribution has been scaled by the known correction factors, to correspond to a coverage of \pm 0.5 in η and 2π in ϕ .

Width of high N_{ch} roll-off is a function of e.g. finite aperture.





First results on centrality dependence of charged particle multiplicity at RHIC energies. If you never wanna see anything more about them pad-chambers:

Avoid NIM A where this 50 page writeup is coming soon at a library near you.

and

WWW/p/draft/andosk/pcnim/final/det_counc/nim_det_counc.ps

Construction and Performance of the PHENIX Pad Chambers

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V. Yurevich^{g,12}

d+Au

Hits/event/plane

West arm, Retracted

No tracking done So some backgnd

ZDC trigg.
No vertex cut.

